IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 6-7, and 14 in accordance with the following:

1. (currently amended) An analog signal control method comprising the steps of:

converting the analog signal to a digital signal via ~~a first path~~ an analog signal process path;

performing an arithmetic processing of the digital signal via the ~~first~~ analog signal process path, to generate a control signal for controlling the analog signal;

delaying the analog signal corresponding to a latency caused by the generation of the control signal to generate a delayed analog signal in ~~a second~~ an analog signal transmission path that is different from the ~~first~~ analog signal transmission path; and

controlling the delayed analog signal in accordance with the control signal in the ~~second~~ analog signal transmission path.

2. (previously presented) The analog signal control method according to claim 1, wherein:

the step of converting the analog signal includes sampling the analog signal at a predetermined sampling timing to generate a sampling value;

the step of generating a control signal includes generating the control signal in accordance with the sampling value; and

the step of delaying includes delaying the analog signal to control the analog signal in accordance with the control signal, the analog signal having the sampling value corresponding to the predetermined sampling timing.

3. (previously presented) The analog signal control method according to claim 1, wherein:

the step of converting the analog signal includes sampling the analog signal at a predetermined sampling timing to generate a sampling value;

the step of generating a control signal includes generating the control signal in

accordance with the sampling value; and

the step of delaying includes delaying the analog signal by a latency equal to or larger than a possible latency to control the analog signal in accordance with the control signal, the analog signal having a sampling value produced by sampling the analog signal at a timing previous to the predetermined sampling timing.

4. (previously presented) The analog signal control method according to claim 1, wherein:

the step of converting the analog signal includes sampling the analog signal at a plurality of predetermined timings to generate a plurality of sampling values;

the step of generating a control signal includes calculating the plurality of sampling values to generate the control signal; and

the step of delaying delays the analog signal to control the analog signal in accordance with the control signal, the analog signal having a sampling value corresponding to an arbitrary sampling timing.

5. (previously presented) The analog signal control method according to claim 1, wherein:

the step of converting the analog signal includes sampling the analog signal at a plurality of predetermined timings to generate a plurality of sampling values;

the step of generating a control signal includes calculating the plurality of sampling values to generate the control signal; and

the step of delaying includes delaying the analog signal to control the analog signal in accordance with the control signal, the analog signal having the plurality of sampling values produced by sampling the analog signal at a timing previous to each sampling timing.

6. (currently amended) An analog signal control method comprising the steps of:

converting the analog signal to a digital signal via ~~a first~~ an analog signal process path;

performing an arithmetic processing of the digital signal via the ~~first~~ analog signal process path, to generate a control signal for controlling the analog signal;

delaying the analog signal corresponding to a latency caused by the generation of the control signal in synchronism with a clock signal to generate a delayed analog signal via ~~a second~~ an analog signal transmission path that is different from the ~~first~~ analog signal process path; and

controlling the delayed analog signal in accordance with the control signal, via the

~~second~~ analog signal transmission path.

7. (currently amended) An analog signal controller comprising:

an ADC for analog-to-digital conversion, the ADC configured to be located in ~~a first~~ an analog signal process path and converting an analog signal to generate a digital signal;

a digital arithmetic circuit located in the ~~first~~ analog signal process path and connected to the ADC for performing an arithmetic processing of the digital signal to generate a control signal for controlling the analog signal;

a delay circuit, located in ~~a second~~ an analog signal transmission path that is different from the ~~first~~ analog signal process path, for receiving the analog signal, and delaying the analog signal corresponding to a latency caused by the ADC and the digital arithmetic circuit to generate a delayed analog signal; and

an analog control circuit, located in the ~~second~~ analog signal transmission path and connected to the digital arithmetic circuit and the delay circuit, for controlling the delayed analog input signal in accordance with the control signal.

8. (original) The analog signal controller according to claim 7, wherein:

the analog signal controller operates in accordance with a clock signal; and

the delay circuit includes a pair of switches which operate complementary to each other in synchronism with the clock signal, and delays the analog signal by switching the pair of switches.

9. (previously presented) The analog signal controller according to claim 8, wherein:

the delay circuit includes a capacitor connected to a node between the pair of switches and a ground.

10. (previously presented) The analog signal controller according to claim 8, wherein:

the delay circuit includes a plurality of delay stages connected in series, each of the delay stages including the pair of switches;

the ADC samples the analog signal to generate a sampling value; and

the delay circuit further includes a selector circuit for selecting a number of connected ones of the plurality of delay stages in accordance with the sampling value of the analog signal.

11. (previously presented) The analog signal controller according to claim 10, wherein:

each of the plurality of delay stages includes a capacitor connected to a node between the pair of switches and a ground.

12. (original) The analog signal controller according to claim 7, wherein:

the delay circuit includes a capacitor for delaying the analog signal; and

the capacitor has a capacitance value which is set such that the analog signal is delayed corresponding to the latency.

13. (original) The analog signal controller according to claim 7, wherein:

the delay circuit includes a variable capacitor for delaying the analog signal; and

the variable capacitor is set such that the analog signal is delayed corresponding to the latency.

14. (currently amended) An automatic gain controller comprising:

a first control loop, located in ~~a first~~ an analog signal process path, for receiving an analog signal to generate a control signal for setting a predetermined gain for use in amplifying the analog signal;

a delay circuit, located in ~~a second~~ an analog signal transmission path that is different from the ~~first~~ analog signal process path, for receiving the analog signal, and delaying the analog signal corresponding to a latency caused by the first control loop to generate a delayed analog signal; and

a gain control amplifier (GCA), located in the ~~second~~ analog signal transmission path and connected to the delay circuit and the first control loop, for amplifying the delayed analog signal in accordance with a predetermined gain set by the control signal to generate an amplified analog signal.

15. (previously presented) An automatic gain controller comprising:

a first control loop, the first control loop including:

a first gain control amplifier (GCA) for amplifying the analog signal in accordance with a first predetermined gain to generate a first amplified analog signal;

an analog to digital converter (ADC) connected to the first GCA for analog-to-digital converting the first amplified analog signal to generate a digital signal;

an error calculating circuit connected to the ADC for calculating an error between a target value which is set such that the first amplified analog signal substantially covers a full range for

an input level of the ADC, and the digital signal to generate an error digital signal in accordance with the error;

a digital to analog converter (DAC) connected to the error calculating circuit for digital-to-analog converting the error digital signal to generate a control signal for setting a second predetermined gain;

a delay circuit for delaying the analog signal corresponding to a latency occurring in the first control loop to generate a delayed analog signal; and

a second GCA connected to the delay circuit and the first control loop for amplifying the delayed analog signal in accordance with the second predetermined gain set by the control signal to generate a second amplified analog signal.

16. (original) The automatic gain controller according to claim 15, further comprising:

a control loop connected to the second GCA for calculating an error for the second amplified analog signal.

17. (original) The automatic gain controller according to claim 15, wherein:

the AGC operates in accordance with a clock signal; and

the delay circuit includes a delay stage for delaying the analog signal in synchronism with the clock signal.

18. (previously presented) The automatic gain controller according to claim 17, wherein:

the delay stage is one of a plurality of delay stages connected in series; and

the delay circuit further includes a selector circuit for selecting the number of connected ones of the plurality of delay stages in accordance with a predictable waveform of the analog signal.

19. (previously presented) An automatic gain controller comprising:

a first analog to digital converter (ADC) for sampling an analog signal to generate a first plurality of sampling values, the first ADC generating a first digital signal in accordance with the first plurality of sampling values;

a first average processing circuit connected to the first ADC for calculating an average value of the first plurality of sampling values in accordance with the first digital signal to generate a first average value signal indicative of the calculated average value;

a first gain selector circuit connected to the first average processing circuit for selecting a

first gain for controlling the analog signal in accordance with the average value of the first average value signal, and generating a first control signal in accordance with the selected first gain;

a first delay circuit for receiving the analog signal, and delaying the analog signal corresponding to a first latency occurring in the first ADC, the first average processing circuit, and the first gain selector circuit to generate a first delayed analog signal; and

a gain switching amplifier connected to the first delay circuit and the first gain selector circuit for amplifying the first delayed analog signal in accordance with the first gain selected by the first control signal to generate a first amplified analog signal.

20. (original) The automatic gain controller according to claim 19, further comprising:

a second AGC connected to the first gain switching amplifier for amplifying the first amplified analog signal, wherein the second AGC includes:

a second ADC for sampling the first amplified analog signal to generate a second plurality of sampling values, the second ADC generating a second digital signal in accordance with the second plurality of sampling values;

a second average processing circuit connected to the second ADC for calculating an average value of the second plurality of sampling values in accordance with the second digital signal to generate a second average value signal indicative of the calculated average value;

a second gain selector circuit connected to the second average processing circuit for selecting a second gain for controlling the first amplified analog signal in accordance with an average value of the second average value signal, and generating a second control signal in accordance with the selected second gain;

a second delay circuit for receiving the first amplified analog signal, and delaying the first amplified analog signal corresponding to a second latency occurring in the second ADC, the second average processing circuit, and the second gain selector circuit to generate a second delayed analog signal; and

a second gain switching amplifier connected to the second delay circuit and the second gain selector circuit for amplifying the second delay analog signal in accordance with the second gain selected by the second control signal to generate a second amplified analog signal.

21. (original) The automatic gain controller according to claim 19, further comprising:

a control loop connected to the first gain switching amplifier for calculating an error of the first amplified analog signal.

22. (original) The automatic gain controller according to claim 19, wherein:

the first average processing circuit changes sampling numbers of the first plurality of sampling values in accordance with a predicted waveform of the analog signal when the waveform of the analog signal is predictable.

23. (original) The automatic gain controller according to claim 19, wherein:

the first average processing circuit changes sampling positions of the first plurality of sampling values in accordance with a predicted waveform of the analog signal when the waveform of the analog signal is predictable.